
This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.

DIVISIONAL
APPLICATION DATA SHEET
FOR
UNITED STATES LETTERS PATENT

APPLICANT NAMES: Joann Alsmeier
Jochen Beintner
Gary Bronner
Ramachandra Divakaruni
Ulrike Gruening
Jack A. Mandelman

TITLE: SELF-ALIGNED NEAR SURFACE STRAP FOR
HIGH DENSITY TRENCH DRAMS

DOCKET NO.: FIS-00-0023DIV

ASSIGNEE NAME: INTERNATIONAL BUSINESS
MACHINES CORPORATION AND
INFINEON TECHNOLOGIES NORTH AMERICA
CORPORATION

ASSIGNEE RESIDENCE: Armonk, New York

SELF-ALIGNED-NEAR-SURFACE-STRAP-FOR-HIGH-DENSITY

TRENCH DRAMS

BACKGROUND OF THE INVENTION

10s A'>

Field of the Invention

5 The present invention generally relates to conductive straps utilized to connect storage devices to transistors and more particularly to self-aligned near surface straps for high density trench storage devices.

Description of the Related Art

Conventional systems for processing trench dynamic random access

10 memory (DRAM) structures form a buried strap by performing two recess steps and etching the collar after the first of these recesses. The second recess provides margin for a dielectric on top of the trench to isolate it from the passing wordline. In this scheme, the buried strap depth (determined by the sum of the first recess and collar wet etch) cannot be made very shallow and is thus not scalable from standard device scaling rules, which as is well known in the art, require shallow junctions. Secondly, the difference in two recess depths combined with the required presence of a thin interface (to prevent dislocations) places severe constraints on the tolerance of the resistance contributed by the buried strap.

Several suggestions have been made to ameliorate some of the problems mentioned above including methods to form the buried strap after active area (AA) definition (which adds considerable cost), a divot strap (which can cause a large pad oxide undercut), and a surface strap (which places considerable pressure on isolation planarization). Therefore, there is a need for a strap that allows better control of the leakage of current from the capacitor and is thus much more scalable.

SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide a structure and method for a dynamic random access memory device comprising a storage trench, a storage conductor within the storage trench, a lip strap connected to the storage conductor, and a control device electrically connected to the storage conductor through the lip strap. The trench contains a corner adjacent the control device and the lip strap and has a conductor surrounding the corner. The control device has a control device conductive region adjacent the trench and the lip strap and has a conductor extending along a side of the trench and along a portion of the control device conductive region. In addition, the device can have a collar insulator along a top portion of the trench, wherein the lip strap includes a conductor extending from a top of the collar to a top of the trench. The lip strap can also extend along a surface of the device adjacent the trench and perpendicular to the trench. A

node dielectric, lining the trench where the lip strap surrounds an upper portion of the node dielectric, is adjacent the top portion of the trench and can have a trench top oxide where the lip strap extends into the trench top oxide and forms an inverted U-shaped structure. Further, the lip strap can include a conductor extending along two perpendicular portions of a top corner of the trench.

The invention further includes a method of forming a dynamic random access memory structure for forming a trench within a substrate, filling the trench with a trench conductor, forming a pad oxide along a surface of the substrate adjacent the trench, forming a collar along an upper portion of the trench such that the collar insulates the substrate from the trench conductor, recessing the collar and the pad oxide, depositing a lip strap over the trench conductor and in recesses produced by the recessing, and forming an isolation region adjacent the lip strap.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

Figure 1 is a schematic diagram depicting a DRAM structure in the formation of the invention;

Figure 2 is a schematic diagram depicting a DRAM structure in the formation of the invention;

Figure 3 is a schematic diagram depicting a section of the collar removed;

Figure 4 is a schematic diagram depicting a near surface strap;

Figure 5 is a schematic diagram depicting a layer of trench top oxide and
pad pull back;

5 Figure 6 is a schematic diagram depicting a completed structure according
to the invention;

Figure 7 is a schematic diagram depicting another lip strap according to
the invention;

10 Figure 8 is a schematic diagram depicting a different aspect of the
invention; and

Figure 9 is a schematic diagram depicting yet another aspect of the
invention.

**DETAILED DESCRIPTION OF PREFERRED
EMBODIMENTS OF THE INVENTION**

15 This invention comprises a method and structure relating to conductive
straps utilized to connect storage devices to transistors and more particularly to
self-aligned near surface straps for high density trench storage devices, the
structure is referred to herein as a near surface or 'lip' strap. The near surface
20 strap is used in the DRAM structures of semiconductor chips or devices and

replaces the conventional buried strap that is typically used with DRAM structures.

The inventive near surface strap provides an electrical connection between a conductor or capacitor in the trench of a DRAM structure and the active devices on the semiconductor chip. While this disclosure will make obvious to those skilled in art other advantages, one benefit of the invention is the formation of a connection between the strap and the conductor that is at the surface of the semiconductor device. This surface connection allows better control of leakage current and, as a result, is much more scalable.

Several embodiments of the invention are discussed below. A first embodiment is shown in Figures 1-6. Conventional DRAM processing well known to those ordinarily skilled in the art is performed until the structure depicted in Figure 1 is formed. The structure includes a substrate 10 (e.g., silicon) having a trench 11 therein. The upper portion of the trench 11 includes an insulating collar 12 (e.g., such as an oxide). A pad oxide 14 extends horizontally from the collar 12 and is positioned between the substrate 10 and a pad 16 which is formed from, for example, silicon nitride. Lining the trench is a node dielectric 18 (e.g., silicon nitride). A conductor 20 (e.g., tungsten, polysilicon,) fills the trench 11. A shallow recess 22 is formed in the conductor 20 down to approximately 20 nm below the upper level 28 of the substrate 10. The recess 22 prevents the conductor 20 from extending above the substrate 10 surface.

PCT/US2003/035002

5

Initially, the invention pulls back (e.g., etches) the node dielectric 18 and the pad 16 so that the collar 12 is exposed, as shown in Figure 2. While the figures illustrate a LOCOS collar, as would be known by one ordinarily skilled in the art, the invention may be easily extended to a conventional TEOS deposited collar. Then, as shown in Figure 3, a strap recess 24 is formed using a wet etch. The oxide may also be etched with anisotropic Reactive Ion Etch (RIE) selective to the pad nitride (16) and silicon (20 and 10). In a preferred embodiment, the strap recess 24 encompasses approximately 20 nm in width and extends from the pad oxide 14 to below the top portion of the node dielectric 18. If the pad oxide 14 has sufficient thickness, the wet etch may create an undercut in the pad oxide 14. In any case, the subsequent fill process discussed below will completely fill any undercut.

10

As shown in Figure 4, the lip strap 26, which can be formed of any suitable conductor, such as polysilicon, tungsten, etc., is deposited and recessed below the pad 16 surface, and above the substrate surface 28. In a preferred embodiment, the "lip strap" 26 extends approximately 20 nm above the upper surface 28 of the substrate 10 as shown by item 27 in Figure 4.

15

20

The shape/size of the lip strap 26 and its height 27 above the substrate surface 28 is governed by the recessing of the lip strap 26. In a preferred embodiment the height 27 of the strap recess is controlled to guarantee that the strap 26 is above the substrate surface 28. When determining the strap recess height 27, the pad 16 thickness variation is important and is considered by the

invention. The appropriate strap recess height 27 may also be controlled using a layered deep trench hardmask process that preserves some oxide (e.g., in a LOCOS process), as would be known by one ordinarily skilled in the art given this disclosure.

5 The pad is pulled back an additional amount as shown in Figure 5, using similar processes as discussed above. In one embodiment, an optional thin trench top (TT) layer 30 (e.g., silicon nitride, etc.) may be deposited on the lip strap 26 to provide a margin for insulation from a passing gate (not shown) on the surface of the pads 16.

10 As shown in Figure 6, a trench top oxide 32 such as tetraethylorthosilicate (TEOS), high density plasma (HDP) oxide, or other suitable insulator, is formed. The trench top oxide 32 is then polished using chemical mechanical polishing (CMP) or other suitable process to planarize the upper surface of the structure.

15 As would be apparent to one ordinarily skilled in the art given this disclosure, the structure can be completed and the active area can be defined using conventional shallow trench isolation (STI), raised shallow trench isolation (RSTI), local the oxidation of silicon (LOCOS), or other similar process.

Figure 7 illustrates one embodiment of the inventive structure after the formation of the isolation region and the gate conductor stacks. More specifically, 20 Figure 7 illustrates the lip strap 26, which is manufactured as discussed above. The resulting RSTI region 70 defines the active area and joins the TTO 32. The pad oxide 14 is replaced with a gate oxide 78, using processes well known to

those ordinarily skilled in the art. The doped source/drain region is illustrated as item 77. Further, the gate conductor stacks include the gate conductor 74, the word line 75 and the nitride caps 76. An insulator 71 such as boron phosphorous silicate glass (BPSG) provides insulation and support. The structure is topped by another insulator, such as TEOS 72.

Figure 7 also illustrates insulating spacers 73, 79. An important feature of the invention is that the insulating spacer 79 is formed adjacent to the TTO region 32. The spacer formation technology is well-known to those ordinarily skilled in the art and will not be discussed in detail here. However, the dielectric spacer 79 can be utilized in a number of different ways to produce different benefits for the invention. More specifically, in one embodiment, the spacers 79 can be formed after the gate sacrificial oxide is stripped and before the gate oxide 78 is grown.

Alternatively, the dielectric spacer 79 can be formed before the pad oxide 14 is stripped. This alternative process would allow the spacer 79 to be densified by the subsequent gate sacrificial oxide growth. This is especially true if the insulating spacer 79 is TEOS based. Further, in an additional embodiment, the spacer 79 could be made of phosphoro silicate glass (PSG) or doped glass. Therefore, in such a situation, the spacer 79 could provide additional dopants to the node junction if needed. Additionally, it is possible to form the spacer 79 as a doped glass spacer after the pad oxide 14 is removed. Then, the dopant could be driven into the node junction when the gate sacrificial oxide is grown. At this point, the doped insulator 79 could be replaced with a pure insulator, if desired.

Subj:

It is to be noted that the structure in Figure 7 may be achieved using

several methods. For example, after the top of the trench is filled with TTO, the
shallow trench isolation (STI) and fill processes are performed. The top of the
trench may be filled concurrently as the STI. The pad nitride is then shipped,
spacers 79 are formed, the gate sacrificial oxide is grown, implants performed, the
sacrificial oxide is shipped, the gate oxide is grown, and the gate polysilicon is
deposited and polished to the TTO (32). The rest of the gate stack is deposited
and the rest of the processing is conventional.

In another example, the structure in Figure 7 can be formed using the
following process. After the top of the trench is filled with TTO as in Figure 6,
the pad nitride is shipped, spacers 79 are formed, the sacrificial oxide gate is
grown, implants performed, the sacrificial oxide is stripped, the gate oxide is
grown, and the gate polysilicon is deposited and polished to the TTO (32). A
fresh pad nitride is then deposited and STI is formed and filled. The pad nitride is
stripped, the rest of the gate stack is deposited and the conventional processing is
then performed to complete the structure.

Another embodiment of the invention is illustrated in Figures 8 and 9.

Figure 8 illustrates a structure which is similar to that shown in Figure 1;
however, the conductor 20 is recessed slightly below the upper surface of the
nitride pad 16, as shown by item 80. This is done to retain the conductor during
the formation of the STI region 93. Then, as shown in Figure 9, the shallow
trench isolation region 93 (and optional liner 92) are formed using conventional

processes and the processes discussed above. After the STI region 93 is formed, the conductor is recessed to level 90 and the lip strap 91 is formed, as discussed above.

Therefore, this embodiment of the invention is substantially similar to the previous embodiments. However, in this embodiment, the STI region is formed before the lip strap 91. By forming the lip strap 91 after the STI region 93, the number of thermal cycles which the lip strap 91 will receive is reduced. Each thermal cycle releases dopants from the conductive lip strap 91. By reducing the number of thermal cycles to which the lip strap 91 is subjected, more dopants are retained within the lip strap 91. This makes the lip strap electrically shallower and increases the device performance accordingly.

Thus, as most clearly shown in Figure 7, the invention is a dynamic random access memory device that includes a storage trench, a storage conductor 20 within the storage trench, a lip strap 26 connected to the storage conductor 20, and a control device 77 (e.g., transistor) electrically connected to the storage conductor 20 through the lip strap 26. The lip strap 26 is a conductor that extends along a side of the trench and along a portion of the transistor 77 conductive region (e.g., source/drain) and, therefore, surrounds a top corner of the trench. The lip strap 26 extends from a top of the collar 12 to a top of the trench and along a surface of the device adjacent the trench and perpendicular to the trench. In other words, the lip strap 26 extends along two perpendicular portions of the top corner of the trench.

SUB 3

As shown in Figure 6, the lip strap 26 surrounds an upper portion of the node dielectric 18 adjacent the top portion of the trench 11. Also, the lip strap 26 extends into the trench top oxide 32 and forms an inverted U-shaped structure within the trench top oxide 32.

5 A major advantage of the last embodiment is that the buried strap 26 is formed after the AA oxidation and thus the invention has a reduced strap out diffusion. All of the embodiments of this invention protect the active silicon in the trench top region from the HDP oxide STI fill. Also, there is no risk of autodoping from the 'lip' to the neighboring active area with the invention. Further, with the invention, the lip strap 26 connection allows better control of leakage current and, as a result, is much more scalable. Further, the processing discussed above the allows the lip strap 26 to be self-aligned, thereby avoiding the inaccuracies and problems associated with lithographic techniques.

10
15 While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.